**Amended Claims**

1. (withdrawn) A LVTSCR-like structure having one or more diodes formed in a p-well of the structure.

2. (previously presented) A method of increasing the holding voltage of a LVTSCR structure that includes an n-well and a p-well formed in a substrate, an n+ region and a p+ region formed in the n-well, and an n+ region and a p+ region formed in the p-well, the method comprising forming at least one additional p+ region and at least one additional n+ region inside the p-well of the structure to define at least one p-n junction between one of p+ regions and at least one of the n+ regions in the p-well that is forward biased during normal operation.

3. (previously presented) A method of increasing the holding voltage of a LVTSCR structure having an anode in an n-well and a cathode in a p-well, the cathode being defined by an n+ region and a p+ region, comprising

forming at least one additional n+ region and at least one additional p+ region in the p-well to define at least one forward biased diode in the p-well, thereby providing an alternative current path from anode to cathode through said at least one diode.

4. (original) A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

**Remarks**:

Claim Rejections – 35 USC 112

Claims 2-4 and 6 were rejected under 35 USC 112 for failing to comply with the written description requirement on the basis that there is no support for the limitation of forming at least one p+ region and at least one additional n+ region inside ~~a~~ the p-well of the structure to define at least one p-n junction between the at least one p+ region and the at least one additional n+ region in the p-well, as claimed in claim 2.

This was addressed in response to the previous Office action. Again, the page and line references will be made to the replacement specification filed with the response that was mailed 9/11/2002 in response to the Office action of 8/12/2002. However, other than the corrections mentioned in that response (corrections to the Field of the Invention line 1, and page 6, line 31 and the adding of the units on page 6, line 31, the content remained the same as at time of filing.

The examiner is referred to Figure 4 of the application and page 8, line 28 – page 9, line 4 which discusses the various p+ and n+ regions, the diodes that they define and the resultant p-n junctions. Thus the inventors clearly had possession of the invention at time of filing.

The examiner repeats his earlier argument that the at least one p+ region and at least one additional n+ region are separated by an isolation region. As described on page 9, lines 1-4 the first p+ region 420 and first n+ region 422 are not isolated – both are formed in a common p-well 402. Charge carriers can freely pass between regions 420 and 422 through the p-well 402. For the oxide region between the p+ region 420 and n+ region 422 to isolate the two regions it would have to extend downward to an isolation layer, which it does not.

In the "Response to Arguments" section, the examiner then states that there is no support for at least one "p-n junction" because a p-n junction requires a direct contact between one p+ region and at least one of the n+ regions.

This is not correct. What is required is that the n+ and p+ regions not be isolated from each other. The p+ region in this case is formed in a p-well which directly contacts the n+ region. The p+ region therefore through the p-well has the necessary contact with the n+ region to define a diode.

Claim Rejections – 35 USC 102

Claims 3-4 were rejected under 35 USC 102 over Ker.

The examiner argues that the claim does not require the structure to have two n+ regions and two p+ regions in the p-well because the additional n+ and at least one additional p+ region need not be different from the previously recited n+ and p+ regions.

It is respectfully pointed out that claim 2 explicitly defines "an n+ region and a p+ region formed in the p-well, the method comprising forming at least one **additional** p+ region and at least one **additional** n+ region inside the p-well of the structure". Under proper claim construction an explicit recitation of an n+ region and a p+ region and an additional n+ and p+ region cannot be interpreted as including just one n+ region and one p+ region.

Since the p-well therefore must include at least two n+ regions and at least two p+ regions in the p-well, Ker cannot be said to teach the specific limitations of the claim. Claim 3 also includes the above limitations that are not present in Ker.

In the event that the examiner believes this not to be the case, applicant requests a formal telephone interview with the examiner and his supervisor in order to discuss the claim limitations.

<u>Claim Rejections – 35 USC 103</u>

Claims 2-4 were also rejected under 35 USC 103(a) over Ker.

It is respectfully submitted that Figures 6, 3a and 4a of Ker do not teach the limitations of claims 2 and 3 of the present application.

As discussed above, claims 2 and 3 positively claim an n+ region and a p+ region in the p-well, and an additional n+ region and at least one additional p+ region in the p-well. Even if the floating N+ region 54 in Ker is defined as one of the n+ regions in the p-well, the p-well still lacks the at least one additional p+ region that the claims of the present application require.

Furthermore, the N+ regions 60 and P+ region 58 of Ker are connected and are therefore at the same potential. They cannot therefore define a forward biased diode. Even N+ region 54 and P+ region 58 are note forward biased since the anode of the device is at a higher potential than the cathode. Thus N+ region 54 would be at a higher potential than the P+ region 58. Thus these two regions would be reverse biased relative to each other.